IN THE CLAIMS:

Please cancel Claims 11-59, without prejudice or disclaimer of subject matter.

The following is a complete listing of claims and replaces all prior versions and listings of claims in the present application:

Claim 1 (original): A computer system, comprising:

a plurality of devices for transmitting bus commands;

a central repeater for broadcasting commands;

a plurality of first uni-directional command bus links for transmitting commands from originating devices to said central repeater;

a uni-directional command bus broadcast portion for broadcasting commands from said central repeater to all devices attached to said command bus;

wherein each of said plurality of first uni-directional command bus links is less wide than said uni-directional command bus broadcast portion, whereby a plurality of bus cycles is required to transmit a command on one of said links, the same command being broadcast from said central repeater in a single bus cycle.

Claim 2 (original): The computer system of claim 1, wherein said system comprises a plurality of processors, at least some of said devices for transmitting bus commands being processors.

Claim 3 (original): The computer system of claim 1, further comprising:

a global command bus arbitrator, said arbitrator granting devices the right to transmit respective commands at respective bus cycles, wherein each command is broadcast by said central repeater a pre-defined number of cycles N after said arbitrator granted the right to transmit the command.

Claim 4 (original): The computer system claim 1, further comprising:

a plurality of local request repeaters, each of said first unidirectional command bus links running from a device to an associated local request repeater; and

at least one second uni-directional command bus link, each of said at least one second links transmitting commands from a local request repeater to said central repeater.

Claim 5 (original): The computer system claim 4, wherein said uni-directional command bus broadcast portion comprises:

a plurality of local broadcast repeaters;

at least one third uni-directional command bus link transmitting commands from said central repeater to said plurality of local broadcast repeaters; and

a plurality of fourth uni-directional command bus links, each of said fourth uni-directional command bus links transmitting commands from a respective local broadcast repeater to at least one device.

Claim 6 (original): The computer system of claim 5, further comprising:

a global command bus arbitrator, said arbitrator granting devices the right to transmit respective commands at respective bus cycles;

wherein each command is transmitted by a device on a first uni-directional link a pre-defined number of cycles N after said arbitrator granted the right to transmit the command, is transmitted by a local request repeater on a second uni-directional link a pre-defined number of cycles M after said arbitrator granted the right to transmit the command, is transmitted by said central repeater on said at least one third link a pre-defined number of cycles L after said arbitrator granted the right to transmit the command, and is transmitted by each of said plurality of local broadcast repeaters on each respective fourth link a pre-defined number of cycles K after said arbitrator granted the right to transmit the command, wherein $N<M<L<K$.

Claim 7 (original): A method for communicating between devices attached to a communication bus in a computer system, said communication bus including a command bus portion, said method comprising the steps of:

requesting control of said command bus portion by a first device attached to said communication bus during a first bus cycle;

receiving a grant of control of said command portion by said first device during a second bus cycle;

transmitting command information for a bus command on a first link of said command bus portion from said first device to a repeater unit during a plurality of consecutive bus cycles beginning with a third bus cycle and ending on a fourth bus cycle, said third and

fourth bus cycles occurring a respective pre-defined number of cycles after said second bus cycle; and

re-transmitting said command information on a second link of said command bus portion from a repeater unit to second device attached to said communication bus during a fifth bus cycle, said fifth bus cycle occurring a pre-defined number of cycles after said second bus cycle, wherein command information transmitted on said first link during multiple cycles is transmitted on said second link in a single cycle.

Claim 8 (original): The method of claim 7, further comprising the steps of:

requesting control of a data portion of said communications bus by said second device during a sixth bus cycle, said sixth bus cycle occurring after said fifth bus cycle, said requesting control of said data portion step being responsive to said bus command;

receiving a grant of control of said data portion by said second device during a seventh bus cycle;

transmitting data on said data portion from said second device during an eighth bus cycle, said eighth bus cycle occurring a pre-defined number of cycles after said seventh bus cycle.

Claim 9 (original): The method of claim 8, wherein said command information includes a tag uniquely identifying said bus command, and wherein said tag is transmitted simultaneously with said data on said data portion.

Claim 10 (original): A processor for use in a multi-processor computer system, said computer system having a communications bus for communicating among processors and memory, said communications bus having a command bus portion for transmitting commands from an originating processor to other devices attached to the communications bus, said processor comprising:

a command bus request port for requesting the right to transmit a command on said command bus portion from an arbitrator;

a command bus grant port for receiving bus grant from said arbitrator;

a command output port having a plurality N of output pins for transmitting bus commands;

a command receive port having a plurality M of input pins for receiving bus commands, wherein M>N, the number of input pins M being sufficient to receive a bus command in one bus cycle; and

interface logic for transmitting bus commands on said command output port responsive to receiving bus grant from said arbitrator, wherein a bus command is transmitted from said plurality of output pins during a plurality of consecutive bus cycles beginning with a first cycle occurring a first pre-defined number of bus cycles after said processor receives bus grant and ending with a second bus cycle occurring a second pre-defined number of bus cycles after said processor receives bus grant.

Claims 11-59 (canceled).